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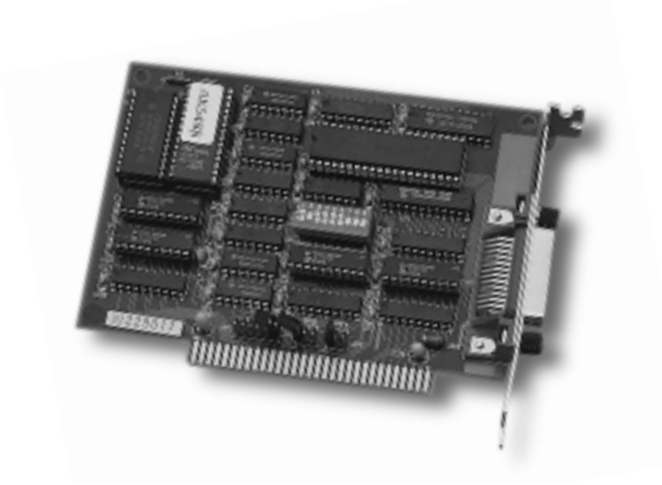
AX5488

GP-IB Interface Board



Features

- Onboard firmware ROM callable for user's application program
- Complete Listener/Talker/Controller (LTC) capability using the NEC μPD7210 GPIB TLC chip
- Data transfer rates over 300K bytes/sec
- Unique hardware features
  - Half-sized board fits any I/O slot
  - RF-shielded IEEE-488 receptable
  - Transparent interrupt enabling /disabling
  - Choice of 6 interrupt lines
  - Transparent DMA channels using host DMA controller
- Shared interrupt capability for compatibility with the IBM™ GPIB adapter
- 6 interrupt levels
- 3 DMA channels
- Call interface routine :
  Supports Basic, Quick Basic, Microsoft C, Turbo C, Turbo Pascal and Microsoft Windows® 3.1&95

General Description

The AX5488 is a full-function IEEE-488 standard GP-IB interface for the IBM™ PC bus. The interface makes possible the transfer of data between thousands of IEEE-488 compatible devices and IBM™ PC/XT/AT or compatible computers.

The AX5488 is a half-sized board that can be plugged into any I/O slot. The AX5488 has the features of shared interrupt capabilities which is compatible with IBM™'s GPIB adapter. IEEE-488 was designed for use in network for instruments, which allows up to 15 devices classified into 3 types: Talker, Listener and Controller.

Application

IBM™ PC equipped with the AX5488 becomes an IEEE-488 controller that can be used for numerous applications in laboratory testing, product testing, and process monitoring and control functions. It can be used to monitor and control medical instruments.

- Data terminal link
- Remote control device interface
- Interfaces PC to other computers or instruments

Specifications

- IEEE-488 B Transfer Rates
  – DMA: over 300 KB/sec
  – Block length: up to 64KB/sec

Power Requirement

- **+5VDC:** 2.0A max.

Physical/Environmental

- **Dimensions:**127 x 107mm
- **Weight:** 250g
- **Relative Humidity:** 0 to 90%, non-condensing
- **I/O Connector:** IEEE-488 standard 24-pin

Programming

Summary of Firmware Routines

Mnemonic	Offset	Description
IBINIT%	0	Initialize the AX5488 driver function routine
IBWRT%	3	Write data string to device
IBRD%	6	Read data string from device
IBIFC%	9	Interface clear to reset GPIB bus
IBEOL%	12	Establish an End of Linestring for I/O of a device
IBDCLR%	15	Clear specified device
IBLLO%	18	Local lockout to disable device front panel operation
IBLOCAL%	21	Make device go to local
IBPPL%	24	Parallel polling
IBPPLC%	27	Parallel polling configure
IBPPLU%	30	Parallel polling unconfigure
IBREN%	33	Set device to remote mode by setting remote enable line
IBCMD%	36	Send command string to device
IBSPL%	39	Serial polling and return device's status
IBSTS%	42	Status of the GPIB bus
IBTOUT%	45	Setup time out interval
IBTRG%	48	Trigger specified device
IBRDM%	51	Read data into memory with specified segment
IBWRTM%	54	Write data from memory to device
IBXCHG%	57	Replace DOS device with GPIB device
IBERR%	60	Return error code

Note: All specifications are subject to change without notice.

Programming Example

The example program shows you how to control HP3478 DMM to measure voltage signals.

```
 10      DEF SEG=&HD000
 20      INIT%=0:IBWRT%=3:IBRD%=6IBRG%=48
 30      HP3478%=23          ' HP3478 address
 40      MYADDR%=21          ' Controller address
 50      IOPORT%=&H2E1
 60      CFG%=&H0003
 70      CALL BINIT%(IOPORT%,MYADDR%, CFG%)
 80      WRTSTR$="F1T3RAN3"        ' Command string
 90      CALL IBWRT%(HP3478%, WRTSTR$)
         ' Write string to HP3478 command
 100     CALL IBTRG%(HP3478%)   ' Trigger HP3478
 110     RDSTR$="          "   ' Space for storing result
 120     CALL IBRD%(HP3478%, RDSTR$)   ' Read
         result from HP3478
130 PRINT "MEASURE=", RDSTR$
```

Hardware Capability

The following paragraphs highlight interface features.

Address Decoding

This circuitry monitors the address lines to recognize when the GPIB I/O address is present on the IBM™ PC I/O channel and enables read and write access to the GPIB interface controller.

Buffering and Data Routing

Bidirectional internal bus handles data transfer between the IBM PC I/O channel and the GPIB inter-face controller.

Interrupt Arbitration

This circuit recognizes when interrupts have been enabled or disabled and passes or inhibits them accordingly.

DMA Arbitration

The DMA arbitration circuit recognizes when DMA operations are enabled or disabled and when the last transfer has taken place. It also routes the DMA request and acknowledges signals to the selected DMA channels.

Configuration Switches and Jumpers

These components determine the I/O port address, the DMA channel pair used, and the interrupt request line used.

GPIB Interface Controller

This integrated circuit, the NEC μPD7210 implements virtually all of the IEEE-488 interface functions. Twenty one program registers are used to configure pass commands and data to and from the GPIB.

GPIB Transceivers

The GPIB interface controller is interfaced to the IEEE-488 bus by National Semiconductor 75160A and 75162A transceivers. These ICs are specifically designed to provide power-up/power-down bus protection (glitch free). The AX5488 counts as one IEEE-488 bus load, thereby allowing an additional 14 devices to be connected before exceeding the bus loading restriction.

Ordering Information

- **AX5488**
  GP-IB Interface Board, including user's manual, Basic ROM drivers and utility diskette with C, Pascal and Windows 3.1 driver

Cable

- **AX10488-0.5**
  GP-IB cable, 0.5 meter
- **AX10488-2**
  GP-IB cable, 2 meter
- **AX10488-1**
  GP-IB cable, 1 meter
- **AX10488-4**
  GP-IB cable, 4 meter

Software Driver

- **AS59021**
  DA&C AX5488 Windows® 95/NT Driver

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